REMARKS

Claims 1-20 are pending in the present application. Claims 1, 2, 3 and 9 are amended above. New claims 21-23 are added above. No new matter is added by the claim amendments or the new claims. Entry is respectfully requested.

The Specification is objected to for reasons indicated in the Office Action. The Specification is amended above. It is believed that the objection to the Specification is overcome, and reconsideration thereof is requested.

The Applicants note that the Office Action Summary does not indicate whether the drawings filed in the application are acceptable. Confirmation of their acceptability is respectfully requested.

The Applicants further note that the Office Action Summary does not acknowledge the claim for foreign priority in the application and does not indicate whether a certified copy has been received. Acknowledgment is respectfully requested.

The Applicants note, with appreciation, that the Office Action indicates at page 4, paragraph 4, that claims 7, 8 and 18-20 would be allowable if rewritten in independent form. With regard to claims 7 and 18, the Applicants wish to defer submission of these claims, pending consideration of the present amendment. New claim 21 is added to incorporate the limitations of former claim 1 and claim 8. New claim 22 is added to incorporate the limitations of former claim 9 and claim 19. New claim 23 is added to incorporate the limitations of former claim 9 and claim 20. Entry and allowance of new claims 21-23 are respectfully requested.

Claims 1 and 9 stand rejected under 35 U.S.C. 102(e) as being anticipated by either Rabinowitz *et al.* (U.S. Patent No. 6,753,812 - hereinafter "Rabinowitz") or Fiscus (U.S. Patent No. 6,492,852). Claims 2-6 and 10-17 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Rabinowitz. Reconsideration of the rejection and allowance of claims 1-20 are respectfully requested.

The present invention as claimed in independent claim 1 is directed to a semiconductor memory device. The semiconductor memory device includes a delay locked loop. Further the semiconductor memory device includes a control signal generator. The control signal generator generates a first control signal at a first output and a second control signal at a second output independent of the first output, which are responsive to a plurality of mode selection signals, each mode selection signal indicative of a mode of operation of the semiconductor memory device. The first and second control signals are operative to turn corresponding first and second portions of the delay locked loop on or off.

The present invention as claimed in independent claim 9 is directed to a semiconductor memory device. The semiconductor memory device includes a delay locked loop. The semiconductor memory device also includes a mode selection signal generator that generates a plurality of mode selection signals. Each mode selection signal is indicative of a mode of operation of the semiconductor memory device. The plurality of mode selection signals are generated in response to operation control signals for controlling operations of the semiconductor memory device. Further, the semiconductor memory device includes a control signal generator that generates a first control signal at a first output and a second control signal at a second output independent of the first output. The first and second control signals respond to the plurality of mode selection signals to turn corresponding first and second portions of the delay locked loop on or off.

In the present invention as claimed in independent claims 1 and 9, a "control signal generator" generates a "first control signal at a first output and a second control signal at a second output independent of the first output". The "control signal generator" generates the first and second control signals "in response to the plurality of mode selection signals". The "mode selection signals" are "indicative of a mode of operation of the semiconductor memory device".

The first and second control signals operate "to turn corresponding first and second portions of the delay locked loop on or off".

Rabinowitz is cited in the Office Action as disclosing a time-gated delay lock loop 940, a controller 942, and "timing signals" provided by the segment modulator 912. The "timing signals" are based on the timing of the code that the segment modulator produces (Rabinowitz, column 14, lines 22-24). The segment modulator 912 produces three segment synchronization signals including a punctual signal 938, an early signal 934, and a late signal 932. The controller 942 creates a signal 944 in response to "timing signals" produced by the segment modulator 912 of the time-gated delay lock loop based on the timing of the code that the segment modulator 912 produces (Rabinowitz, column 14, lines 18-23). The signal 944 turns the time-gated delay lock loop on and off, such that the memoryless elements are only operational and producing signals when those signals are needed (Rabinowitz, column 14, lines 18-22).

Rabinowitz fails to teach or suggest "a first control signal at a first output and a second control signal at a second output independent of the first output", as claimed in claims 1 and 9. Rather, Rabinowitz teaches a control signal 944 at a single output. In addition, Rabinowitz fails to teach or suggest the first and second control signals operative "to turn corresponding first and second portions of the delay locked loop on or off", as claimed in claims 1 and 9. Instead, Rabinowitz utilizes only a single control signal 944 for turning only one portion ("memoryless elements") on or off. Rabinowitz further fails to teach or suggest a "plurality of mode selection signals, each mode selection signal indicative of the mode of operation of the semiconductor memory device" in response to which the "first and second control signals" are generated, as claimed in claims 1 and 9. Instead, Rabinowitz teaches generating the single control signal 944 based on the "timing signals" that are indicative of the timing of the time-gated delay lock loop. Therefore, it is believed that amended independent claims 1 and 9 are allowable over Rabinowitz. Reconsideration of the rejection of claims 1 and 9 under 35 U.S.C. 102(e) as being anticipated by Rabinowitz is respectfully requested.

Fiscus is cited in the Office Action as disclosing a delay locked loop, a pre-divider 116 that outputs a control signal to turn off the delay chain 105, and a post-divider 114. When the delay locked loop is in a locked state, the interlock operations of the pre- and post-dividers are enabled (Fiscus, column 6, lines 51-53). The pre- and post-dividers operate mutually exclusive of each other such that if the pre-divider is enabled, such as when the memory device is in an idle state, the post-divider is disabled (Fiscus, column 6, lines 59-62). An interlock switch is used to automatically switch between the pre- and post-dividers based on whether the memory banks are in an idle state (Fiscus, column 6, line 62 - column 7, line 7).

Fiscus fails to teach or suggest a "a first control signal at a first output and a second control signal at a second output independent of the first output" (emphasis added) that operate "to turn corresponding first and second portions of the delay locked loop on or off", as claimed in claims 1 and 9. In Fiscus, the pre- and post-dividers are enabled or disabled on a mutually exclusive basis in response to the same signal (i.e., output of the interlock switch). In addition, Fiscus fails to teach or suggest generating the first and second control signals "in response to the plurality of mode selection signals"(emphasis added), as claimed in claims 1 and 9. Instead, the Fiscus signal that enables or disables the pre- and post-divider is generated in response to a single state, i.e. idle state, of the memory device. Therefore, it is believed that the amended independent claims 1 and 9 are allowable over Fiscus. Reconsideration of the rejection of claims 1 and 9 under 35 U.S.C. 102(e) as being anticipated by Fiscus is respectfully requested.

It is therefore submitted that independent claims 1 and 9 are in condition for allowance, and such allowance is respectfully requested. With regard to the various dependent claims, it follows that these claims should inherit the allowability of the independent claims from which they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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